WHAT IS CLAIMED IS:

1. A control circuit within a UART, comprising:

an input for receiving a half duplex mode enable signal, which half duplex mode enable signal causes said UART to operate in a half duplex mode of operation and in a full duplex mode of operation;

at least one input for receiving at least one signal indicating whether there is data for the UART to transmit; and

circuitry for disabling a receiver port of said UART, which circuitry is coupled to said input for receiving said half duplex mode enable signal, which circuitry is also coupled to said at least one input for receiving at least one signal, and which circuitry also has an output coupled to said receiver port of said UART to enable said receiver port to receive.

2. The UART control circuit of claim 1, wherein said at least one input includes an input from a FIFO register set for carrying a FIFO empty signal received indicating that there is no data in the FIFO register set for transmission by the UART.

3. The UART control circuit of claim 2, wherein said output only enables said receiver of said UART to receive

whenever a half duplex mode enable signal is not received and whenever a half duplex mode enable signal is received and said FIFO empty signal received from said FIFO register set indicates that there is no data in the FIFO for transmission.

4. The UART control circuit of claim 3, wherein said at least one input also includes an input from a data store for carrying a data store empty signal indicating that there is no data within said data store for transmission by the UART.

5. A UART control circuit of claim 4, wherein said output only enables said receiver of said UART whenever said half duplex mode enable signal is not received and whenever said half duplex mode signal is received, and said FIFO empty signal from said FIFO register set indicates that there is no data in the FIFO register set and whenever said FIFO empty signal received from the data store indicates that there is no data in the data store for transmission by the UART.

6. The UART control circuit of claim 5 which further comprises an input from a processing unit indicating whether a UART receiver enable flag has been set wherein said UART control circuit output only enables said receiver whenever

said input from said processing unit indicates that said UART receiver enable flag has been set.

7. A UART for single channel communications, comprising:

a transmission data store coupled to receive data for an external source, which transmission data store is for storing data for transmission by said UART as a signal;

a transmitter port for transmitting signals;

a transmission data register set for temporarily holding up to a predefined amount of data for transmission by said transmitter port, which transmission data register set is coupled to receive data from said transmission data store and is coupled to transmit data to said transmitter port;

a receiver port for receiving transmitted signals;

a receiver data store coupled to said receiver port to receive data representation of said received transmitted signals;

a processor unit for controlling UART operations; and

a logic unit coupled to said receiver port and to said transmission data store and transmission data register

set for enabling and disabling said receiver port at select times.

8. The UART of claim 7 wherein said logic unit further includes an input for receiving a half duplex mode enable signal, which input is coupled to an external device.

9. The UART of claim 8 which further includes an input for receiving a UART receiver enable flag, which input is coupled to said processing unit.

10. A method, in a UART which includes a data store for transmitting the FIFO, a transmitter, a receiver, a data store for receiving, data input and output lines, and an input for controlling mode, the method comprising the steps of:

determining if said input for controlling mode of operation specifies a half duplex mode of operation;

determining if said transmitter FIFO is empty;

determining if said transmit data store is empty;

enabling said receiver to receiver if said half duplex enable mode is being specified and if said transmit FIFO and data store are both empty;

and enabling said receiver to receive if said half duplex mode of operation is not being specified; and

disabling said receiver when said half duplex mode is being specified and said transmit FIFO is not empty and disabling said receiver when said half duplex enable mode is being specified and said data store is not empty.

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